What is claimed is:

1. A method for combining adjacent subchannels in a signal processing system having at least two adjacent subchannels, comprising the steps of:

providing a first linear phase digital filter and a second linear phase digital filter in each adjacent subchannel, where the first and second linear phase digital filters are implemented using digital circuitry having a plurality of registers;

adding a delay to one of the first and second linear phase digital filters in each adjacent subchannel, such that the delay is equal to the delay associated with one register in the digital circuitry; and

summing the two adjacent subchannels, thereby forming a composite channel having linear phase.

2. The method of Claim 1 wherein the step of providing a first linear phase digital filter and a second linear phase digital filter further comprises configuring the first and second linear phase filters in a cascade form.

3. The method of Claim 1 wherein the step of providing a first linear phase digital filter and a second linear phase digital filter further comprises using finite impulse response (FIR) filters.

4. The method of Claim 3 wherein the step of providing a first linear phase digital filter and a second linear phase digital filter further comprises the steps of implementing one of the first and second linear phase filters using a Parks-McClellan design technique and implementing the other of the first and second linear phase filters by duplicating the one linear phase filter implemented using the Parks-McClellan design technique.

5. A method for implementing a digital multi-channel frequency channelizer, comprising the steps of:

determining a polynominal form that is indicative of a prototype filter;

computing a polyphase decomposition for the prototype filter in order to derive at least two adjacent filter channels, where each adjacent filter channel includes two linear phase digital filters which are implemented in digital circuitry having a plurality of registers;

adding a delay to one of the two digital filters in each of the adjacent filter channels, such that the delay is equal to the delay associated with one register in the digital circuitry; and

combining the two adjacent filter channels, thereby forming a frequency channelizer having linear phase.

6. The method of Claim 5 wherein the step of determining a polynominal form further comprises defining the prototype filter as a finite impulse response (FIR) filter.

7. The method of Claim 5 wherein the step of determining a polynominal form further comprises using a Parks-McClellan design technique to realize the prototype filter.

8. The method of Claim 5 wherein the step of computing a polyphase decomposition further comprises configuring the two linear phase digital filters in a cascade form.

9. A method for combining adjacent subchannels to form a composite channel having linear phase, comprising the steps of:

providing a first finite impulse response (FIR) filter and a second FIR filter in a first subchannel, where the first and second FIR filters exhibit linear phase and are implemented in digital circuitry having a plurality of registers;

adding a delay to one of the first and second FIR filters, such that the delay is equal to a delay associated with one register in the digital circuitry;

providing a third FIR filter and a fourth FIR filter in a second subchannel, where the third and fourth FIR filters exhibit linear phase and are implemented in the digital circuitry;

adding a delay to one of the third and fourth FIR filters, such that the delay is equal to the delay associated with one register in the digital circuitry; and

summing the first and second subchannels, thereby forming a composite channel having linear phase.

10. The method of Claim 10 further comprising the steps of:

providing a fifth and a sixth FIR filter in a third subchannel, where the fifth and sixth FIR filters exhibit linear phase and are implemented in the digital circuitry;

adding a delay to one of the fifth and sixth FIR filters, such that the delay is equal to the delay associated with one register in the digital circuitry; and

summing the third subchannel with the composite channel to form a second composite channel having linear phase.